## REMARKS

The Examiner has restricted the claims to one of the following inventions under 35 U.S.C. 121:

I. Claims 59-95, drawn to a memory device.

II. Claims 1-45, drawn to a method of making a memory device.

III. Claims 46-58, drawn to an apparatus.

As indicated above, Applicant elects, without traverse, Group II, claims 1-45. Claims 46-95 have been canceled.

## CONCLUSION

Applicant respectfully requests a favorable examination of the merits of this patent application. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 10 day of July, 2005.

Tina Kolnik
Name

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Signature

housing the integrated circuit in a vapor etch chamber; and

vapor phase etching an insulator layer formed adjacent to a double-sided capacitor container in the integrated circuit, wherein the vapor phase etching of the oxide layer comprises inserting a vapor comprised of a hydrogen fluoride and isopropyl alcohol into the vapor etch chamber.

17. (Original) The method of claim 16, further comprising heating the hydrogen fluoride and the isopropyl alcohol prior to inserting the vapor into the vapor etch chamber.

18. (Original) The method of claim 16, wherein vapor phase etching the insulator layer formed adjacent to the double-sided capacitor container in the integrated circuit comprises vapor phase etching a doped oxide layer formed adjacent to the double-sided capacitor container in the integrated circuit.

19. (Original) The method of claim 16, wherein vapor phase etching the insulator layer formed adjacent to the double-sided capacitor container in the integrated circuit comprises vapor phase etching a borophosphosilicate glass (BPSG) layer formed adjacent to the double-sided capacitor container in the integrated circuit.

20. (Original) The method of claim 16, wherein inserting the vapor comprised of hydrogen fluoride and isopropyl alcohol into the vapor etch chamber comprises inserting the vapor comprised of hydrogen fluoride, isopropyl alcohol and an etch initiator composition into the vapor etch chamber.

21. (Original) A method comprising:

placing a substrate that includes an array of memory into a chamber, the array of memory having at least one memory container with a side wall with an embedded capacitor; and